AMENDMENTS TO THE CLAIMS

Claims 1-4, 7-9, 12-18, 21, 25, and 29-31 have been amended, and new claims 32-38 have been added. The following is a complete listing of the claims, which replaces all previous versions and listings of the claims.

1. (currently amended) A method for transacting between an initiator device and a plurality of target devices, the method comprising ~~the steps of~~:

configuring the plurality of target devices to associate a portion of memory with a particular target device of the plurality of target devices;

sending a multicast transaction from the initiator device to the plurality of target devices;

executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target device.

2. (currently amended) The method of claim 1, ~~the configuring step further~~ comprising:

assigning a base memory address to be shared by the plurality of target devices; and

assigning a first portion of memory to a first target device of the plurality of target devices.

3. (currently amended) The method of claim 2, wherein the transaction is a read request for a block of stored data from memory, ~~the executing step further~~ comprising:

reading the base memory address from the read request;

initiating a read operation by the plurality of target devices assigned to the base memory address;

fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device; and

sending the fetched data to the initiator device.

4. (currently amended) The method of claim 2, wherein the transaction is a write request for data to be stored in memory, ~~the executing step further~~ comprising:

reading the base memory address from the write request;

initiating a write operation by the plurality of target devices assigned to the base memory address; and

writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device.

5. (original) The method of claim 1, wherein the target devices comprise input/output controllers.

6. (original) The method of claim 1, wherein the target devices comprise disk array controllers.

7. (currently amended) The method of claim 1, wherein the plurality of target devices comprise a target group[[,]] ~~the target group~~ addressable with a single base memory address.

8. (currently amended) The method of claim 1, ~~further~~ comprising[[:]] a plurality of target groups.

9. (currently amended) A method for transacting data stored in memory between an initiator device and multiple target devices, the method comprising ~~the steps of~~:

detecting a multicast transaction request;

accessing a first portion of memory by a first target device ~~associated with the first portion of memory~~ in response to the multicast transaction request; and

accessing a second portion of memory by a second target device ~~associated with the second portion of memory~~ concurrently with the access to the first portion of memory in response to the multicast transaction request.

10. (original) The method of claim 9, wherein the target devices comprise input/output controllers.

11. (original) The method of claim 9, wherein the target devices comprise disk array controllers.

12. (currently amended) The method of claim 9, wherein the first target device and the second target device are ~~configured as part of a target group, the target group~~ addressable with a single base memory address.

13. (currently amended) The method of claim 9, ~~12, wherein~~ comprising a plurality of target devices ~~are~~ configured into multiple target groups, wherein each of the multiple target groups is addressable with a single base memory address.

14. (currently amended) The method of claim 9, wherein the multicast transaction comprises ~~is~~ a multicast read request.

15. (currently amended) The method of claim 9, wherein the multicast transaction comprises ~~is~~ a muiticast write request.

16. (currently amended) A computer system for communicating between an initiator device and multiple target devices comprising:

a communications bus;

an initiator device coupled to the communications bus, the initiator device configured to initiate ~~for initiating~~ a transaction request; and

a plurality of target devices coupled to the communications bus, wherein each of the plurality of target devices concurrently executes ~~for executing the transaction request, the plurality of target devices executing the transaction request by each target device concurrently responding to~~ a portion of the transaction request.

17. (currently amended) The computer system of claim 16, wherein the plurality of target devices comprise input/output controllers.

18. (currently amended) The computer system of claim 16, wherein the plurality of target devices comprise disk array controllers.

19. (original) The computer system of claim 16, wherein the plurality of target devices are accessed with a single base memory address.

20. (original) The computer system of claim 16, wherein the plurality of target devices comprise a target group.

21. (currently amended) The computer system of claim 20, ~~further~~ comprising[[:]] a plurality of target groups.

22. (original) The method of claim 16, wherein the transaction is a multicast read request.

23. (original) The method of claim 16, wherein the transaction is a multicast write request.

24. (original) The computer system of claim 16, wherein the communications bus comprises a Peripheral Component Interconnect (PCI) bus.

25. (currently amended) A computer system for multicast input/output transactions, comprising:

a processor;

a communications bus coupled to the processor;

an initiator device coupled to the communications bus, the initiator device configured to issue ~~for issuing~~ a multicast transaction; and

a plurality of target devices coupled to the communications bus, the plurality of target devices configured to execute ~~for executing~~ the multicast transaction with concurrent interleaved data responses.

26. (original) The computer system of claim 25, wherein the target devices comprise input/output controllers.

27. (original) The computer system of claim 25, wherein the target devices comprise disk array controllers.

28. (original) The computer system of claim 25, wherein the plurality of target devices comprise a target group, the target group addressable with a single base memory address.

29. (currently amended) The computer system of claim 28, ~~further~~ comprising[[:]] a plurality of target groups.

30. (currently amended) The method of claim 25, wherein the multicast transaction comprises ~~is~~ a multicast read request.

31. (currently amended) The method of claim 25, wherein the multicast transaction comprises ~~is~~ a multicast write request.

32. (new) A computer comprising:

a memory;

a controller configured to logically divide the memory into a plurality of interleaved memory regions; and

a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request.

33. (new) A method comprising:

dividing a section of memory into a plurality of interleaved memory regions;

associating the plurality of interleaved memory regions with a plurality of target devices;

associating the plurality of target devices with a single base memory address; and

executing a memory access that simultaneously involves each of the plurality of target devices accessing the interleaved memory region associated with each of the particular target devices.

34. (new) The method of claim 33, wherein executing the memory access comprises executing a read operation.

35. (new) The method of claim 33, wherein executing the memory access comprises executing a write operation.

36. (new) A tangible machine readable medium comprising:

code to initialize a plurality of devices;

code to configure the plurality of devices to associate a base address with the plurality of devices; and

code to assign each of the plurality of devices a portion of an interleaved memory space.

37. (new) The tangible medium of claim 36, comprising:

code to issue a single read command comprising the base address;

code to recognize the base address as associated with the plurality of devices;

code to simultaneously execute a plurality of memory requests involving the plurality of devices;

code to receive data from the plurality of devices; and

code to write the received data to a communications bus.

38. (new) The tangible medium of claim 36, comprising:

code to issue a write command comprising the base address;

code to recognize the base address as associated with the plurality of devices; and

code to simultaneously write to the plurality of devices.